Claims

[c1] What is claimed is:

1.A method for recording power failure time of a computer system, the computer system comprising:

a power supply for generating a power signal;

a first memory for recording data; and

a processor for processing data comprising:

a power port connected to the power supply for receiving the power signal;

an input port for receiving a power good signal; and

an output port connected to the first memory for outputting the power failure time of the computer system to the first memory;

the method comprising following step:

(a)when the input port of the processor does not receive the power good signal, and the power signal has dropped below a threshold voltage , then the processor writes a first power failure time and a first check number into the first memory, the first check number being calculated by using the first power failure time.

[c2] 2.The method of claim 1 wherein the memory is a non-volatile RAM (random access memory).

[c3] 3.The method of claim 1 wherein the first power failure time and the first check number are written into the first memory before the power signal drops to a minimum operation voltage of the processor, the threshold voltage being above the minimum operation voltage.

[c4] 4.The method of claim 1 further comprising following step:

(b)if the power good signal is still not received, and the power signal is still below the threshold voltage, then the processor writes a second power failure time and a second check number into the first memory, the second check number being calculated by using the second power failure time.

[c5] 5.The method of claim 1 further comprising following step:

(c)after the processor is reset, the power failure time corresponding to a selected check number is read out from the first memory in the memory and is

written into a second memory.

[c6] 6.The method of claim 1 further comprising following step:
(d)writing a power back time into a second memory after the processor is reset.

[c7] 7.The method of claim 6 wherein the power failure time and the power back time are written according to a real time clock (RTC).

[c8] 8.The method of claim 7 wherein the real time clock is provided by a component selected from a group consisting of a processor and a south bridge.

[c9] 9.The method of claim 1 wherein the power signal is a standby power signal.

[c10] 10.The method of claim 1 wherein the computer system further comprises a logic circuit for generating the power good signal, the input port of the processor being connected to the logic circuit for receiving the power good signal.

[c11] 11.A computer system comprising:
a power supply for generating a power signal;
a first memory for recording data; and
a processor for processing data comprising:
a power port connected to the power supply for receiving the power signal;
an input port for receiving a power good signal; and
an output port connected to the first memory for outputting the power failure time of the computer system to the first memory;
wherein when the input port of the processor does not receive the power good signal, and the power signal has dropped below a threshold voltage , then the processor writes a first power failure time and a first check number into the firstmemory, the first check number being calculated by using the first power failure time.

[c12] 12.The computer system of claim 11 wherein the memory is a non-volatile RAM (random access memory).

[c13] 13.The computer system of claim 11 wherein the first power failure time and the first check number are written into the first memory before the power signal

drops to a minimum operation voltage of the processor, the threshold voltage being above the minimum operation voltage.

[c14] 14.The computer system of claim 11 whereinif the power good signal is still not received, and the power signal is still below the threshold voltage, then the processor writes a second power failure time and a second check number into the first memory, the second check number being calculated by using the second power failure time.

[c15] 15.The computer system of claim 11 wherein after the processor is reset, the power failure time corresponding to a selected check number is read out from the first memory in the memory and is written into a second memory.

[c16] 16.The computer system of claim 11 wherein after the processor is reset, a power back time is written into a second memory.

[c17] 17.The computer system of claim 16 wherein the power failure time and the power back time are written according to a real time clock (RTC).

[c18] 18.The computer system of claim 17 wherein the real time clock is provided by a component selected from a group consisting of a processor and a south bridge.

[c19] 19.The computer system of claim 11 wherein the power signal is a standby power signal.

[c20] 20.The computer system of claim 11 further comprising a logic circuit for generating the power good signal, the input port of the processor being connected to the logic circuit for receiving the power good signal.